

# TAPAS - A P4 compiler for a variety of targets

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## Multi-target P4 compiler framework

### T4P4S Compiler

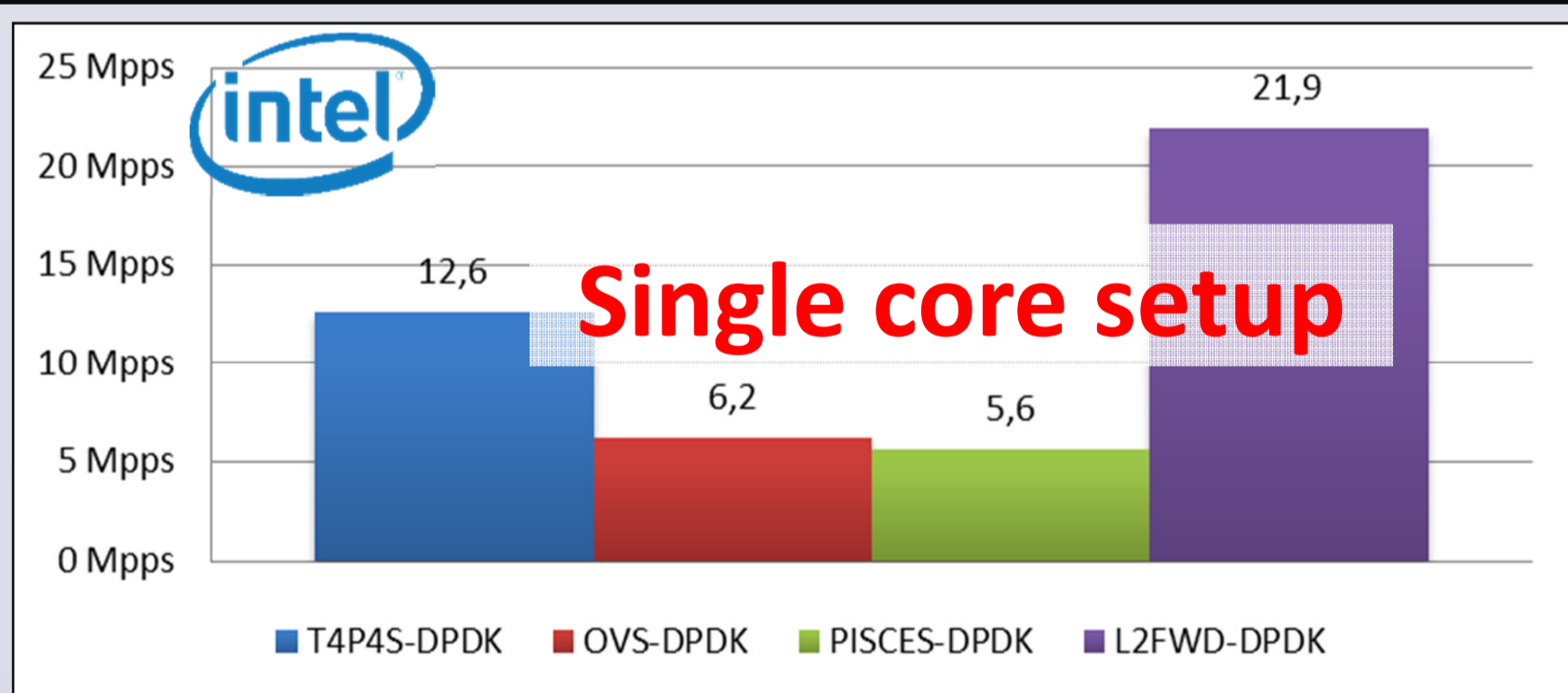
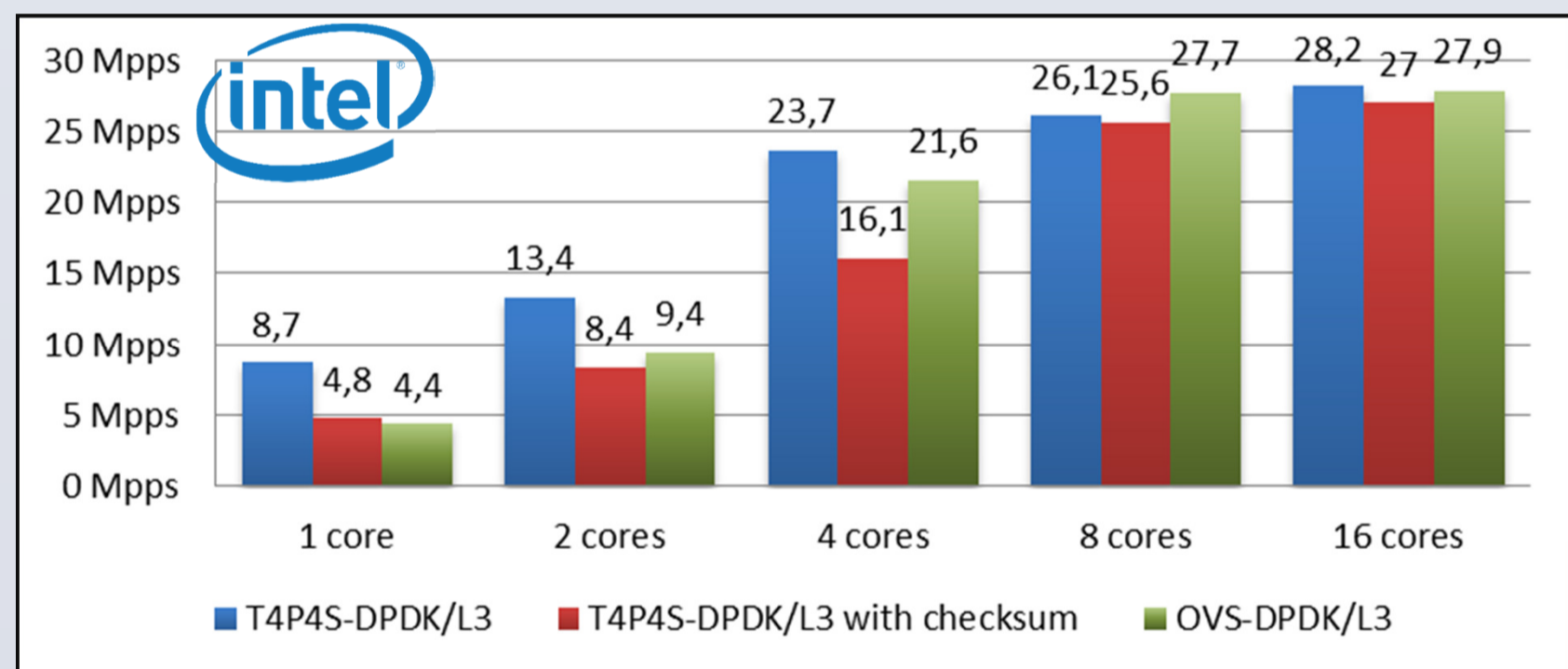
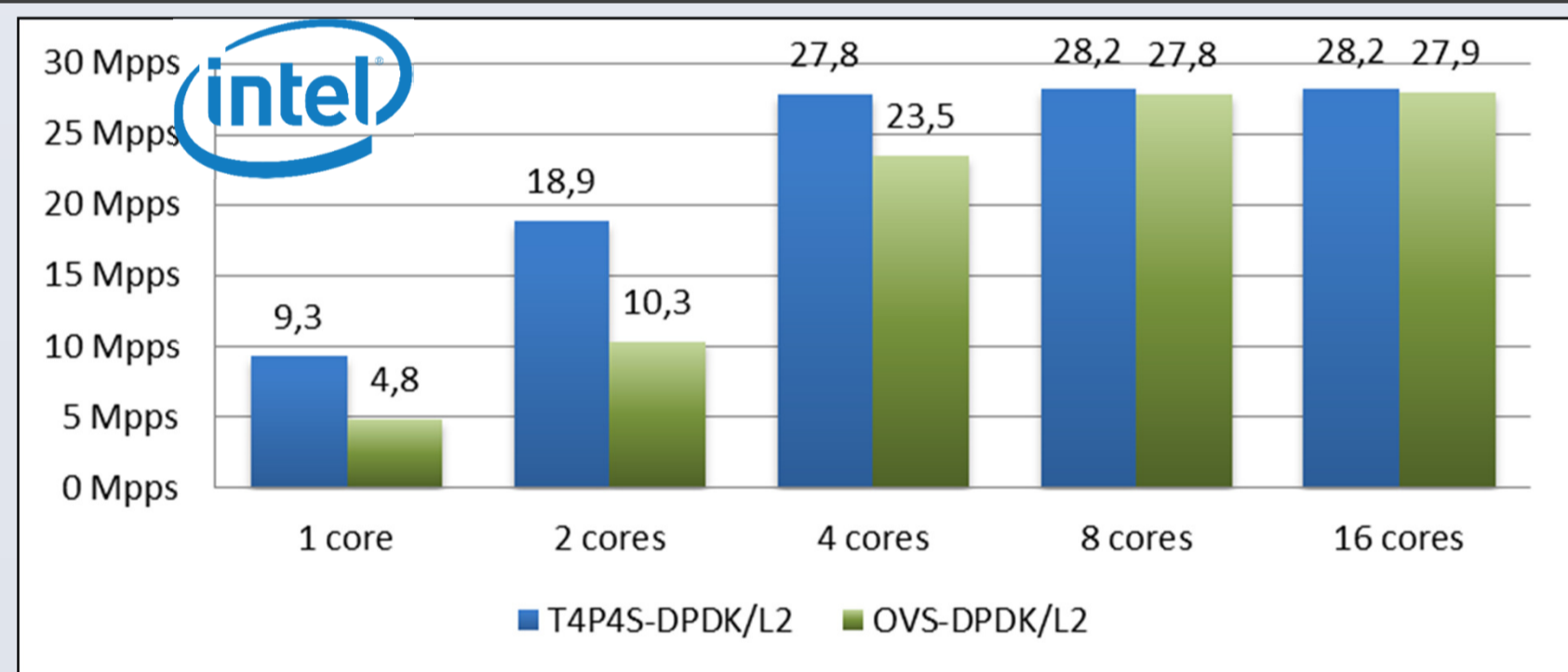
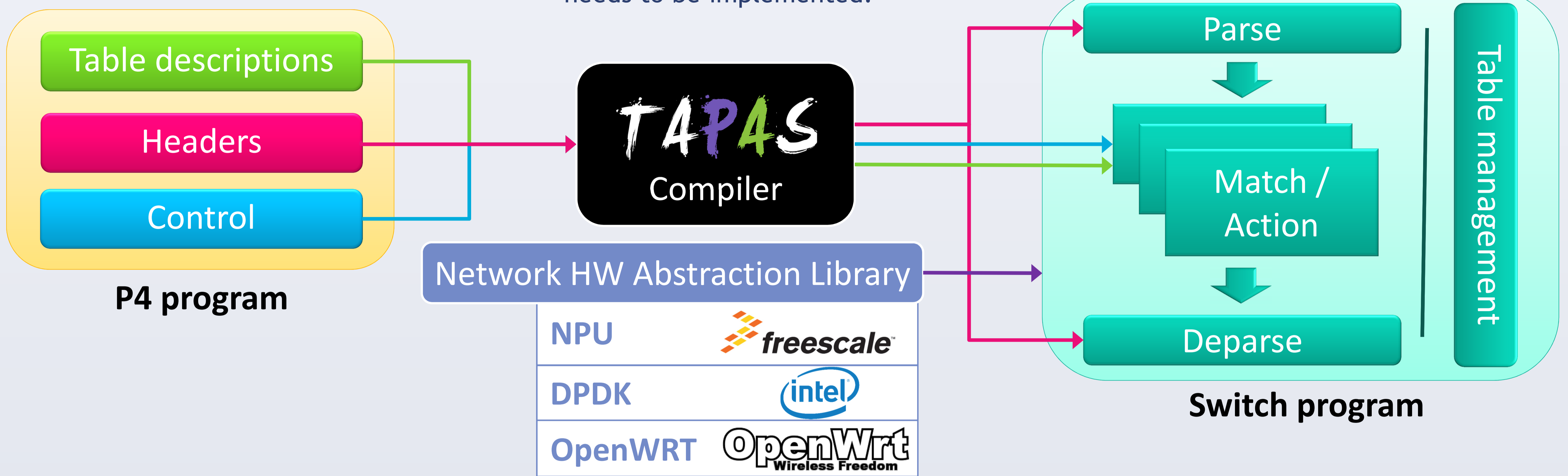
Our retargetable compiler (T4P4S - Translator for P4 Switches) turns a P4 code into a target independent C core program running on the top of a Network Hardware Abstraction Library (NetHAL).

### NetHAL

Hardware dependent operations are separated to the Network Hardware Abstraction Library (NetHAL) which improves portability: to support a new architecture, only a new NetHAL needs to be implemented.

### Switch program

To run the core program on a specific hardware the appropriate NetHAL needs to be linked. The compiled switch program then parse incoming packets, apply match-action rules and deparse messages before egressing.



## Performance measurements

### Scenario 1: Intel DPDK target

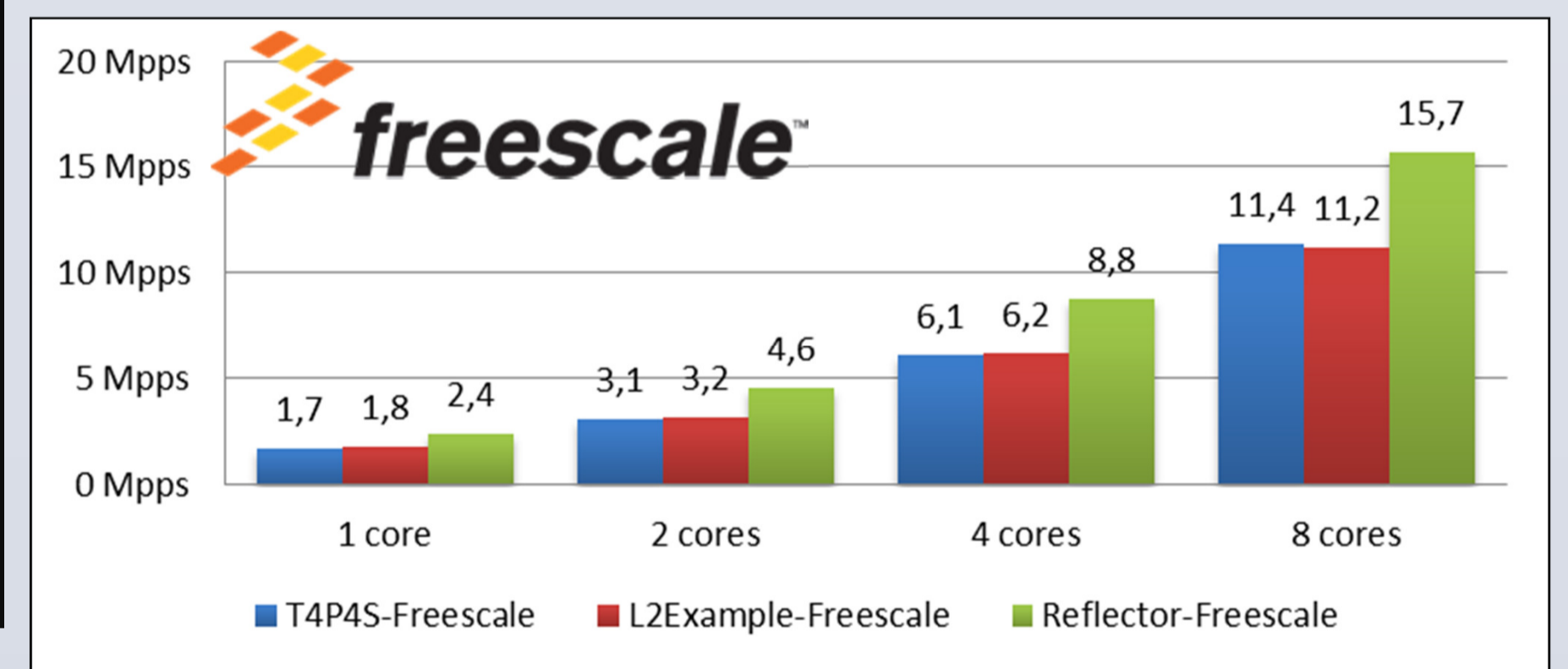
- Two examples - test traffic with packet size 64B
  - Simple L2 forwarding - smac and dmac tables with 200 entries in each
  - Simple L3 forwarding - ipv4\_lpm and nexthop tables with 200 entries in each
- P4 and OpenFlow (OVS) implementations
- Similar testbed setup as the demo setup below
  - Intel Xeon CPU E5-1660 v4 @ 3.20GHz 8C 16T
  - 64GB RAM
  - 60Gb/s Mellanox cards (MT27700 Family)

### Scenario 2: Intel DPDK target

- Simple L2 forwarding as Scenario 1
- P4, OpenFlow and native dpdk implementations
- Similar testbed setup as the demo setup below
  - Intel(R) Xeon(R) CPU E5-2680 v3 @ 2.50GHz
  - 40Gb/s Intel cards (XL710 for 40GbE QSFP+)

### Scenario 3: Freescale ODP-SDK target

- Simple L2 forwarding as Scenario 1
- Comparison to L2 example and Reflector implementations
- Similar testbed setup
  - Traffic generator: Intel DPDK pktgen
- P4 switch node
  - Freescale QorIQ LS2045A board (8 x Cortex-A57 CPUs, 64-bit, 2 GHz, 2x8GB DDR4 RAM)



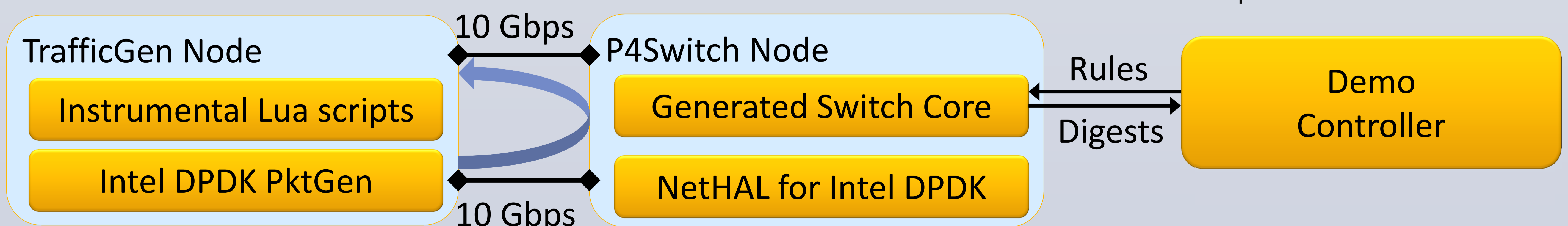
## Demo setup

Small testbed deployed at Eötvös Loránd University with 2 nodes

- Intel Core i5-650 Processor, 2C/4T, 4MB cache, 3.2 GHz, 4GB RAM
- Intel Corporation 82599ES 10-Gigabit Dual port NIC
- DPDK 16.07

Use cases

- L2 forwarding with 2 tables
- L3 forwarding with 3 tables
- NAT example



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